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... 13 **VHDL** Verilog HardwareC Communicating Sequential Processes (CPS ... **process** P begin variable x; ... **SEND** (x); ... end ... Q begin variable y; ... **RECEIVE** (y); ... end ...

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## A Simplified VHDL UART

... UART (Universal Asynchronous Receiver Transmitter) in **VHDL** and download ... TXD 2 3 0 Transmit Data RXD 3 2 i **Receive** Data RTS ... Modify main.c to **send** each character ...

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## IPPT7 Real-Time embedded Systems

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... channels carry messages. **send** and **receive** actions. ... ||. P3:: recv m2 from P1; **send** m3 to P2. ... Various Languages employ this. HW description languages (**VHDL**, **Verilog**). ...

[www.cse.iitb.ac.in/~ramesh/IT-606-ramesh-1.2.ppt](#) - [Similar pages](#)

## IPPT7 Communication and Synchronization Using Bounded Channels in SUAVE

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... For example, in **Verilog** [12, 18], data types are ... we have developed extensions to **VHDL** to improve ... that information is transferred using the **send** and **receive** ...

[www.cs.adelaide.edu.au/users/esser/publications/suave-hdlcon-99.pdf](#) - [Similar pages](#)

## IPPT7 VHDL - Practical Example - Designing an UART

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... Expert Douglas HDL Instructor (**Verilog-VHDL**) info@ALSE ... Standard & 100% portable **VHDL**

Description : - Synthesis ... type State\_Type is (Idle, Get, **Send**); signal State ...

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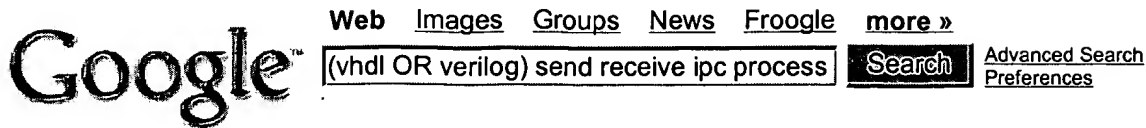
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... module hardware process1 hardware process2 **Verilog** PLI software ... routines Socket **IPC**  
 Refined **VHDL** model with ... d) d) • Synchronization – **IPC** (Inter-Process ...  
[poppy.snu.ac.kr/~kchoi/class/sys\\_des/sys05\\_cosim.pdf](http://poppy.snu.ac.kr/~kchoi/class/sys_des/sys05_cosim.pdf) - [Similar pages](#)

**[ps] An Integrated Hardware-Software Cosimulation Environment for ...**File Format: Adobe PostScript - [View as Text](#)

... a distributed network using Cadence **Verilog**-XL simulator ... To **send(receive)** data to(from)  
 the hardware ... The software and **VHDL** simulationprocesses communicate each ...  
[poppy.snu.ac.kr/papers/ASPDAC95.ps](http://poppy.snu.ac.kr/papers/ASPDAC95.ps) - [Similar pages](#)  
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**[PDF] Cosimulation II**File Format: PDF/Adobe Acrobat - [View as HTML](#)

... **VHDL** Simulator VEC Interface to Software Bus C program ... of a single simulator (say  
**Verilog**) there is ... receiveData() •sendData() Block objects **send** and **receive** ...  
[courses.cs.tamu.edu/rabi/cpsc689/lectures/lecture12/cosimulation2.pdf](http://courses.cs.tamu.edu/rabi/cpsc689/lectures/lecture12/cosimulation2.pdf) - [Similar pages](#)

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... deterministic For example when a **process receive** at the ... passing processes communicatethrough  
 messages **send** with a ... we will concentrate on the **VHDL** gen eration ...  
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**[PDF] ÒÒ Ð ×ØÖ Ø ÓÒ Ò ÈØ Ø Ñ ÒØ Ä Ú Ð ÓÒ ÙÖÖ Ò ...**File Format: PDF/Adobe Acrobat - [View as HTML](#)

... .. init A; **send** A(x); ... init A; **receive** A(y ... vpp .vhdl .vhdl Design file Internal  
 representation generator Parsing .vhdl .vhdl .vhdl INPUT: OUTPUT ...  
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... Unit integrated as an IP-block at the **VHDL**-level ... terminate, etc), inter-**process** com-  
 munication (**IPC**, message **send/receive**), synchronisation (semaphores ...  
[www.mrtc.mdh.se/publications/0378.pdf](http://www.mrtc.mdh.se/publications/0378.pdf) - [Similar pages](#)

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... that performs technology mapping of RT-code (described in **VHDL** or **Verilog**). ... Condition  
 Message Token Based Blocking **Receive** Non Blocking **Send** Data Deadlock ...

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... event time For example Synopsys VSS VHDL simulator provides ... cosimulation In mode we allow to **send** the simultaneous ... guarantee that it will not **receive** any past ...

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... Design VHDL & Verilog ASIC Emulation ... Comment concerning "one-directional" in pipe\_create caused initial confusion that processes could **send** or **receive** ...

[www.vanteon.com/experience/ite/ATC%20API%20Working%20Group%20Presentation.pdf](http://www.vanteon.com/experience/ite/ATC%20API%20Working%20Group%20Presentation.pdf) - [Similar pages](#)

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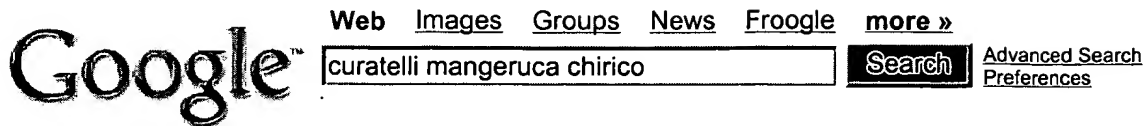
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... Data communication management in system specification.

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